The Complete Readout System for THz Spectroscopy

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***Abstract*—This paper deals with design of readout system, and then its monolithic implementation, intended for spectroscopy in THz range. At the beginning, the fundamentals of THz spectroscopy based on selective NMOS pixel line, and its possible applications for materials identification are presented. Next, the preceding work on single-channel readout circuit is shortly recalled, with a special emphasis on the last design version featuring selective chopper amplifier. This IC became the basis of the complete readout system addressed in next few sections of this paper. Finally, design of novel integrated circuit is presented, incorporating the multi-channel readout circuit dedicated for pixel line.**

***Index Terms*—Terahertz Spectroscopy, Terahertz NMOS-based Detector, Chopper Amplifier, Integrated Readout Circuit, Readout System, AVR ATMega.**

I. Introduction

Nowadays, newly elaborated optoelectronic sensors introduce significant improvements in many domains of security, also including the detection of explosive materials [1]. In this context, terahertz range of electromagnetic spectrum seems to be very interesting because of fingerprints of different substances [2]. Low energy of THz radiation corresponds well with weak bonds and bending or rotational modes of molecules [3]. Many dangerous materials (RDX, TNT, HMX, etc.) have absorption peaks in this range [1], [2], [4], as it is illustrated in Figure 1.

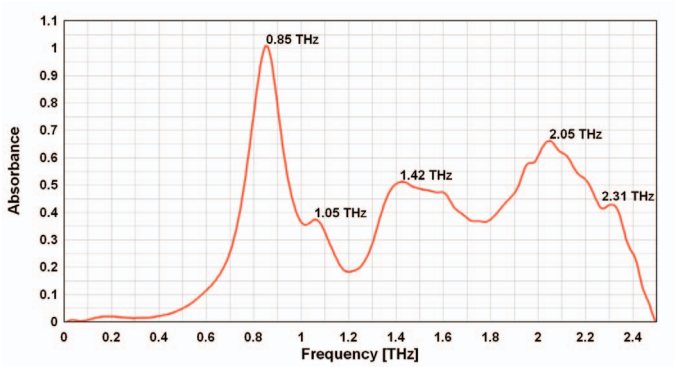

Fig. 1. Absorption curve of RDX

These spectral features give us possibility to distinguish one substance from another. The fact that many textile materials are transparent for THz radiation [5] is also very important for security applications. These two reasons allow people to think about a stand-off detection and identification of hidden explosives [6]. Unfortunately, commercially available spectrometers are expensive and fragile systems. One of the ways to avoid those obstacles is to use spectrally selective detectors dedicated for a given material. Such a detectors can be arranged as monolithic collection of detecting NMOS transistors, integrated with on-chip patch antennas tuned to discrete set of frequencies within interesting range, as described in [7].

II. Readout Amplifier for Single NMOS THz Detector

The essential component of the complete readout system being the main subject of this paper is the single-channel integrated readout circuit. The full process of design, simulation and measurement of this IC was presented in details in [8] & [9]. This work recalls only its principles, essential to fully understand operation of the complete multi-channel readout system.

The single-channel readout circuit is based on well-known *chopper amplifier* concept, its architecture is schematically shown in Figure 2.

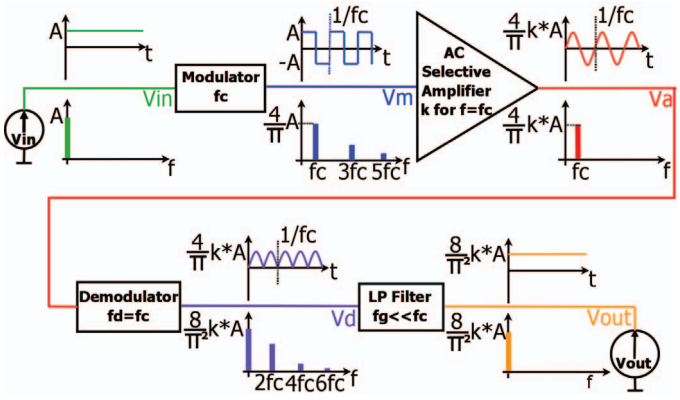

Fig. 2. Architecture of designed single-channel readout amplifier with signals illustrated in time and frequency domains [9]

Low DC voltage signal from detector (V_{in}) is modulated and converted to square wave (V_m) of $f_c = 200kHz$ frequency.

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Then, next block provides amplification of the fundamental frequency component (200 kHz) and suppression of the other ones. This results in sine wave (V_a), which is afterward rectified (V_d) and filtered (V_{out}). The major advantages of such approach are significant 1/f noise reduction - because only single AC component is amplified, and very good output noise parameters due to bandpass limitation. Both are of the key importance when processing small DC signals.

Modulator and demodulator are just simple switching circuits, composed of four CMOS switches each. Selective AC amplifier is a BP filter, based on $G_m - C$ architecture, with gyrators simulating appropriate inductance. The LP filter implements the unity-gain Sallen-Key low-pass architecture. More details about each component have been described in [9].

The table below summarizes the most important parameters of the single-channel readout IC.

TABLE I
MAIN PARAMETERS OF THE SINGLE-CHANNEL AMPLIFIER

PARAMETER	VALUE
Bandwidth	0... 3.875 kHz
Gain	18.2/38.2/58.2 dB
Input impedance (at 100 Hz)	27 $M\Omega$
Input noise density (at 100 Hz)	22 $\frac{nV}{\sqrt{Hz}}$
Output SNR (with detector connected to input)	57 dB

The input spectral noise density curves shown in Figure 3 illustrate the vast advantage of chopper amplifier architecture utilized in design - significant reduction of 1/f noise component.

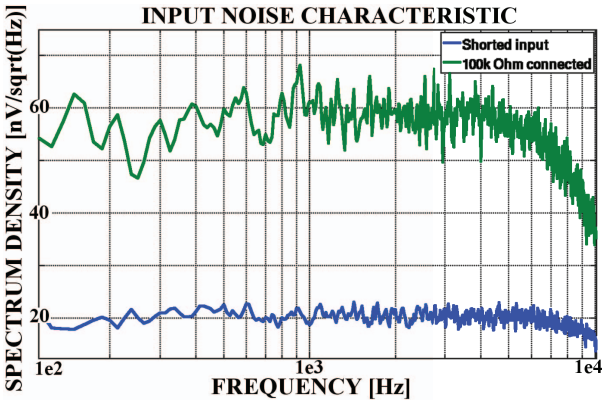

Fig. 3. Input noise spectral density of single-channel amplifier for shorted input (blue) and connected 100 $k\Omega$ resistor (green) [9]

III. READOUT SYSTEM FOR THZ SPECTROSCOPY

Upon successful completion of measurement process for the selective, single-channel readout circuit, it was decided to focus on the solution dedicated for a pixel line. Prior to starting the work on its monolithic implementation, the system called demonstrator was constructed as a proof of concept, to check and confirm design assumptions intended for further implementation in silicon. The number of channels supported by demonstrator circuit was limited to eight, what is the typical size of pixel lines designed and manufactured in ITE proprietary silicon process.

A. The System Architecture

One of the main issues in process of designing multichannel readout circuit was the right choice of the split point within the circuit signal path - decision on what part of the circuit should be common, and what should be kept individual for each channel. Simple switching of detectors to one, common, single-channel readout circuitry is impractical due to distortion caused by the switching process, dominating the very small signal produced within detecting NMOS. Another reason is relatively high time constant of the connected together high output impedance of the detector (several hundreds of kiloohms) and switch capacitance, resulting in a very low switching frequency obtainable. To achieve satisfactory circuit parameters while keeping its area cost moderate it was decided to introduce the channel switching (multiplexing) just after the first gain stage succeeding modulator. In this point, the signal amplitude is high enough, and the output impedance of the stage preceding multiplexer is sufficient, to guarantee negligible level of distortions and reasonable switching frequency. Another important question concerns minimization of crosstalk between channels. To address this issue, the clocking signal is generated only for active (chosen) modulator, while all remaining ones are switched off, hence the output products of inactive modulators are only DC. This would dramatically reduce the effects of parasitic capacitive coupling.

Figure 4 presents simplified architecture of designed readout system.

B. System Design Details

Taking under consideration that testing of the eight channel readout circuit would require simultaneous control of several analog and digital signals (e.g. detector bias, offset settings, modulator clocking, channel selection) it was decided to build the demonstrator in extended form of a system consisting of digitally controlled measurement unit, supervised from microcontroller-based control unit. Instead of starting from scratch, eight single-channel readout circuits, described in [9] were used to build the signal path for each particular channel. The modulated signal after traversing the first gain stage is available via auxiliary (testing) output, and then passed through external (PCB level) multiplexer. The remaining part of the signal path - demodulator and second gain stage is also build of the single-channel readout IC - the ninth one. The signal from analog multiplexer is passed through its input, with modulator clocking switched off, hence it reaches the gain stage preceding demodulator, without any changes. It is important to notice, that in this solution, the signal path designed inside single-channel readout IC as differential one, was converted to single ended, because of using the only one available input for demodulator - normally connected to detecting NMOS. To address the problem of potential DC offset increase, the set of differential amplifiers switched by

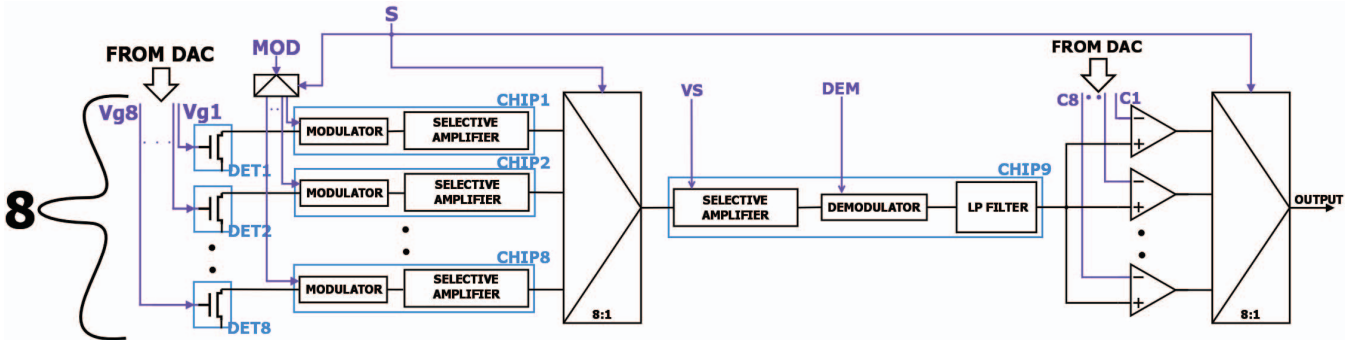

Fig. 4. Simplified architecture of designed readout system

channel selection signal was added at the output. The offset compensation voltages are generated within the 10-bit octal DAC.

From the mechanical point of view, the measurement unit is built inside the shielding enclosure and consists of three PCBs, stacked and interconnected with pin headers. The bottom PCB contains two octal, 10-bit digital to analog converters, used for pixel biasing (gate to source voltages) and for offset compensation at the output, respectively. The 12-bit ADC is used for the output signal measurement, which is also available at the buffered analog BNC output. Three converters share common, precise, thermally compensated reference voltage source, however, the reference for ADC is produced with voltage divider to better match the expected signal range. The sensitive signal path is located at the upper PCB with its bottom layer acting as a shield. The signal tracks are separated by grounded ones to minimize the crosstalk. The nine single-channel readout ICs were assembled to the PCB using chip-on-board technology instead of typical ceramic packages, to reduce the occupied area and PCB tracks length and to facilitate putting them inside additional shielding enclosure. The pixel line, assembled on small PCB is placed at the middle of upper board and connected using DIL24-400 socket. Special attention is paid to elimination of interferences conducted through supply lines - the power tracks for the small signal analog parts are routed separately, and connected together in one star point, next to the positive and negative voltage regulators at the bottom PCB. The supply for switching part of the readout ICs and clocking signal generator is decoupled using Π topology LC filters. The components of clocking signal generator and modulator-to-demodulator phase shifter are located at the bottom side of the lower PCB and shielded with its upper side metal filler. The measurement unit is fitted with rechargeable battery to be fully insulated from interferences conducted by power line. The supply is switched on from the system controller unit using miniature relay. The digital interface providing control signals and data exchange between measurement unit and system controller is also fully galvanic separated by means of fast optocouplers.

The interesting functionality of the measurement unit is related to its auxiliary output intended for oscilloscope triggering. It can be driven with the modulation frequency or the channel switching signal to facilitate the measurements performed on direct, analog output of the readout circuitry.

C. System Controller

The role of system controller is to supervise the operation of measurement unit, to set the analog outputs of its DACs and to gather and present actual output data. This block is based on a ATMega 32 microcontroller (Atmel 8-bit AVR RSIC family), equipped with two lines character LCD and local keypad.

The embedded program supports following operations:

- Definition of new pixel line. The newly defined lines are automatically marked with subsequent numbers. This menu item allows to define gate-to-source voltages for all pixels within the line and to store such a sets of values in nonvolatile memory.
- Modification of pixel line - used to adjust or rewrite settings of already defined line.
- Reading the line definition from memory - allows to use one of already defined pixel lines.
- Definition of offset values - intended to compensate the output offsets of each particular readout channel.
- Choosing the pixel selection (scanning) mode: manual or automated. In manual scanning mode, the index of active pixel is set from local keypad.
- Frequency setting for automated pixel selection (scanning) mode. User can chose one of 5 predefined scanning frequencies.
- Triggering output mode. Within this menu item user can activate the auxiliary output of measurement unit and drive it with modulation or channel switching frequency. Useful for analog measurements on direct output
- Activation of display and keypad backlight. Intended for measurements in dark room.

The system controller is also designed to play the role of interface between PC running application developed for use with NI LabVIEW^{TM} and measurement unit. For this kind of operation it is fitted with USB transceiver. It is worth to mention that serial link intended for communication with measurement unit is also utilized to upgrade the embedded software of system controller without the need of its disassembly.

IV. Readout System for THz Spectroscopy - Measurements

The initial, functional tests of proposed measurement system were performed using replacement source of variable, small DC signal, based on two thermocouples, as described in [8]. The inputs for subsequent pixels were connected to the source by voltage dividers with 1, 1/2, 1/3, 1/4, 1, 1/2 ,1/3 and 1/4 ratios, to simulate staircase stimuli signals from the pixel line. Having obtained the positive test results, the next measurement was performed at the Institute of Optoelectronics of Military University of Technology in Warsaw. The test environment is shown in Figure 5.

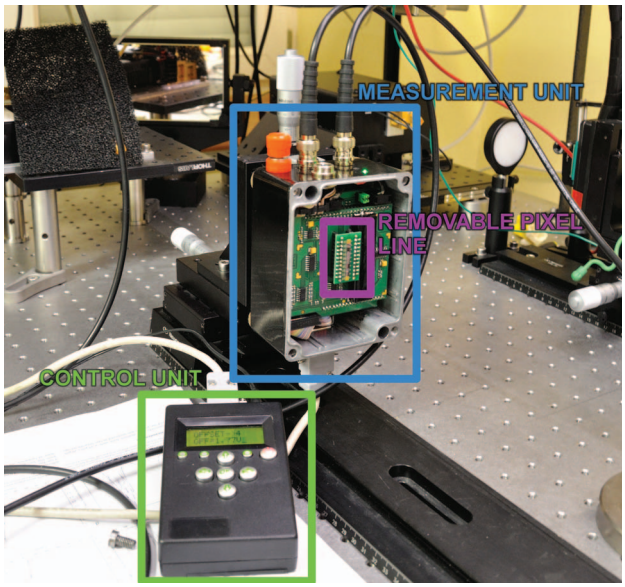

Fig. 5. Test environment at Institute of Optoelectronics (Military University of Technology)

Measurement was carried out with detecting line made of 8 single pixels of the same type. Figure 6 presents results obtained in automated pixel scanning mode (frequency set to 10 Hz), with THz beam (340 GHz) centered in-between the fourth and fifth pixels. The upper waveform shows the output signals from subsequent pixels (detectors), denoted by numbers above the trace. In this way the power distribution within THz beam, in vertical direction is illustrated. The lower waveform in the figure is signal from triggering output of the measurement unit, 5 times wider pulse indicates the first pixel.

V. Dedicated IC for Designed Readout System

The system presented and described in section III contains in its signal path nine previously fabricated single-channel chips and several of-the-shelf components, like operational amplifiers, octal multiplexers and passives. The aim of designing the multi-channel readout IC was to encapsulate all these components into a single monolithic structure, to minimize the system. The split point of the signal path - place where multiplexer is inserted - is the same as in described

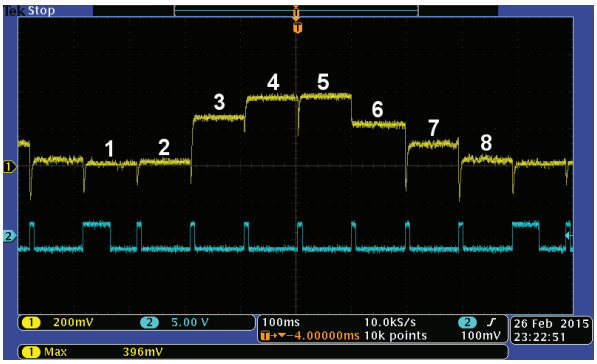

Fig. 6. Measurement of 8-pixel line, THz beam centered in-between the fourth and fifth pixels

demonstrator circuit. The schematic view of the IC structure is shown in Figure 7.

In the system presented in section III each gain stage was based on the same bandpass $G_m - C$ structure. In discussed IC the variable selective amplifier (see Figure 7) implements the second-order Sallen Key *Multiple Feedback Topology*. Main advantage of this architecture is the ability to change the gain without an impact on the other important circuit parameters like bandwidth and quality factor. This can be achieved by switching the resistor network connected to the operational amplifier. Designed selective amplifier is characterized by gain equal to 20/40dB, central frequency 200kHz, 3dB-bandwidth 22.8kHz and quality factor 8.8. Another significant improvement in respect to the demonstrator presented in III is related to offset compensation. Unlike in single-channel IC and demonstrator system, each channel is fitted with differential input pair. One, positive input of each channel is connected to detecting NMOS, while the second one can be driven by offset compensation network. This feature is intended for implementation of the autocalibration procedure: first, both inputs of each particular channel are shorted together and output voltage is measured to determine the offset value, then proper compensation voltage is applied at negative input of each channel. Procedure can be repeated for better accuracy.

Other blocks presented in Figure 7 are similar to corresponding components used in the previously designed chip (see section II).

Transient simulation results are presented in Figure 8.

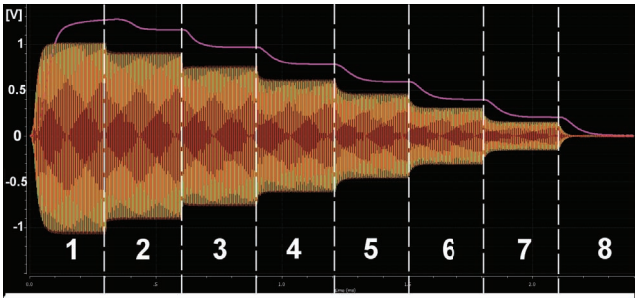

Fig. 8. Transient simulation results: IC DC output (pink) and sine traces before demodulator (red&green)

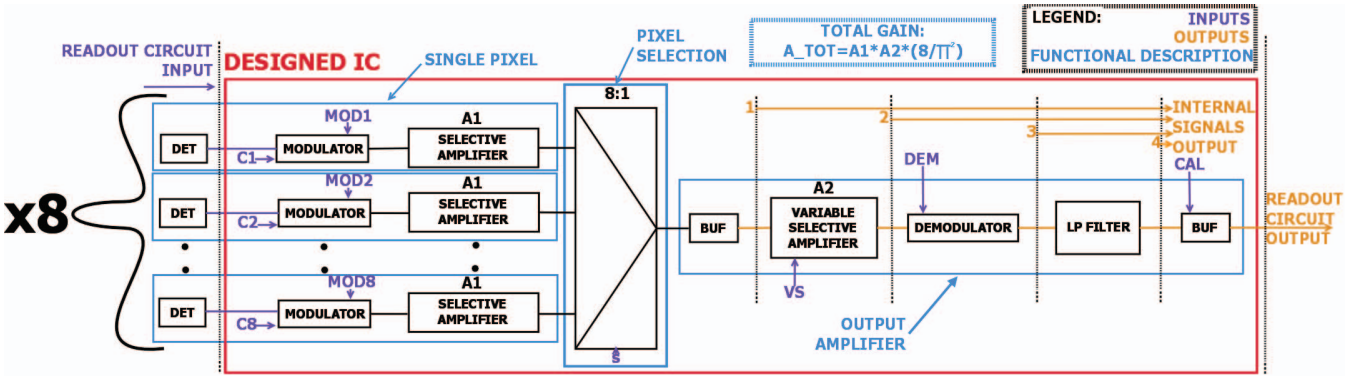

Fig. 7. Overall view of designed IC architecture

Readout circuit was connected, at the testbench level, to the eight different voltage sources simulating THz detectors output signals. Their amplitudes were arranged in descending order - for better results visualization. The channel switching process was performed with 0.3ms period. There are three traces shown in Figure 8: one is the DC output signal and the remaining two are complementary sine waves before the demodulator block (see Figure 7). The indices of detectors are placed under the waveform. Noticeable delay at the circuit output is the result of significant time constant of the output LP filter.

Designed IC was fabricated in AMS C35 process, layout is presented in Figure 9 (4 X 2.5 [mm]). Like in previously designed chips ([8], [9]) all structures are isolated from external radiation by grounded metal 4 layer.

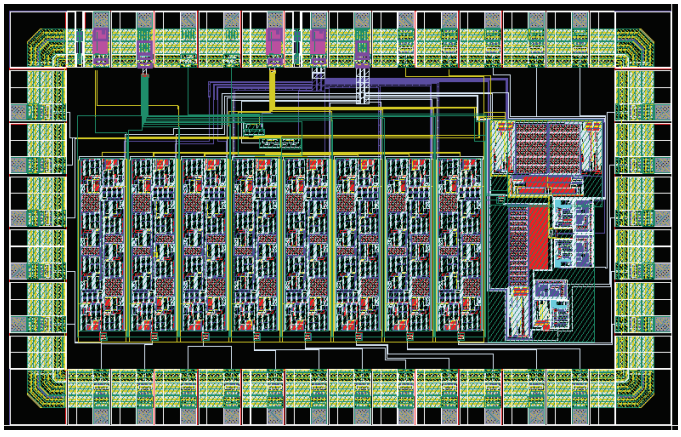

Fig. 9. Layout of integrated readout system

VI. Dedicated IC for Designed Readout System - Measurements

A. Test Setup

The test setup for monolithic, multi-channel readout circuit was developed with totally different design aims than demonstrator, coming from different applications of mentioned systems. Having in mind that full characterization of the circuit requires the noise parameters and crosstalk measurements to be performed, special attention was paid to minimize the reception of external interferences, as well as to limit the noisy digital part of the test setup to clocking signal generators only.

The test setup, illustrated in Figure 10, is fully shielded in a metal enclosure, with battery power supply located inside. Typical design practices like supply line separation, careful decoupling and current flow directing in metal fill layers were applied to minimize parasitic coupling and interferences propagation. For crosstalk, and dynamic (switching characteristic) measurements, the four of eight signal input pairs are available at the front panel. The special circuit block is added to enable experiments with input and output offset compensation. The IC under test is assembled in LCC44 package.

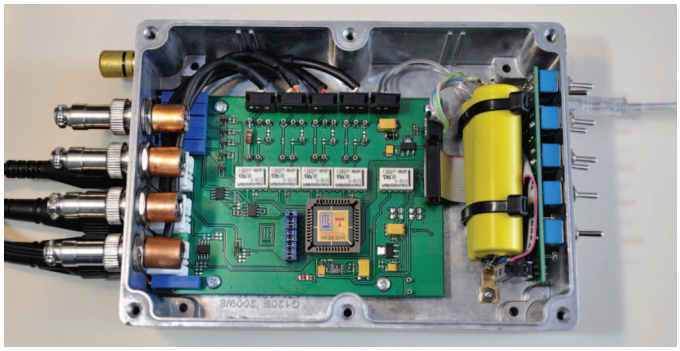

Fig. 10. Test setup for measurements of the readout IC (top cover removed)

B. Measurements Results

The test setup described above has been used to perform the characterization of developed IC. The internal signals of the IC, available via test outputs (see Figure 7 for reference) are presented in Figure 11. The measurements are in perfect matching with theory and simulations.

The exemplary transfer characteristics for one channel of the readout circuit are shown in Figure 12. The gain can be switched (60/80 [dB]) by means of the vs control signal.

It is important to mention that there is also a possibility to affect the gain by manipulating the chopping frequency (signal controlling modulator and demodulator circuits). The characteristics shown in Figure 12 were taken for f_{chop} = 209kHz,

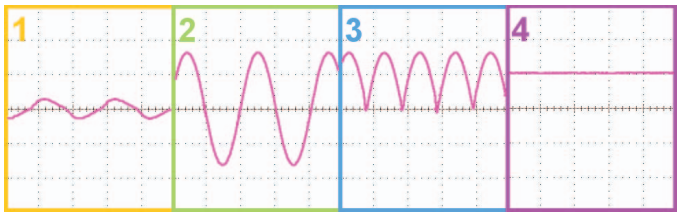

Fig. 11. Internal signals from multi-channel IC: 1 - after multiplexer; 2 - after 2nd gain stage; 3 - after demodulator; 4 - after LP filter

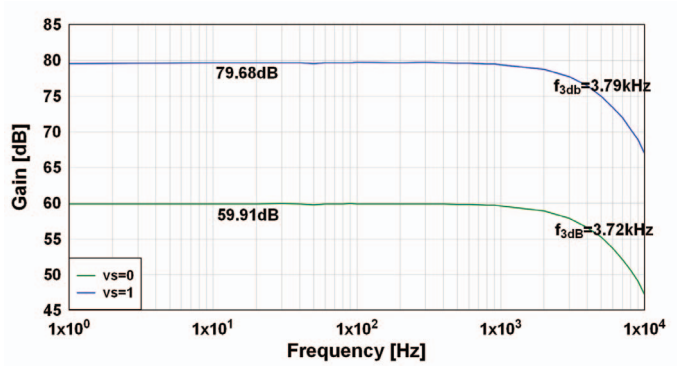

Fig. 12. Transfer curve for channel #0, depending on the vs control signal

resulting in maximum gain. The relation between chopping frequency and the gain is illustrated in Figure 13 - the center frequency (max gain) is marked as f_c. While modifying f_{chop}, a special attention must be payed to the phase shift between demodulator and modulator control signals (MOD and DEM in Figures 4 & 7). For $f_{chop} = f_c$ this shift is equal to 0 and is increasing with rising chopping frequency.

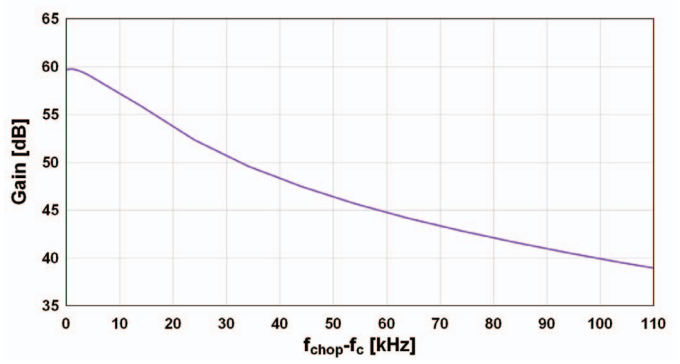

Fig. 13. Relation between f_{chop} and the circuit gain

Figure 14 presents the input noise density curve, taken for three different configurations: with both differential inputs shorted to the ground and with the $100k\Omega/200k\Omega$ resistors connected between them. Presented results once again proves the main advantage of the chopper amplifier architecture - significant reduction of the 1/f noise component.

VII. Conclusions

The complete, digitally-controlled, multi-channel readout circuit aimed at THz spectroscopy was designed and successfully tested by authors. After confirmation of its design assumptions, the extended replacement of its signal path was implemented in silicon. This dedicated IC has been successfully measured and tested, the achieved results are in perfect matching with simulations. The final design step will be related to monolithic implementation of the complete system, including data converters.

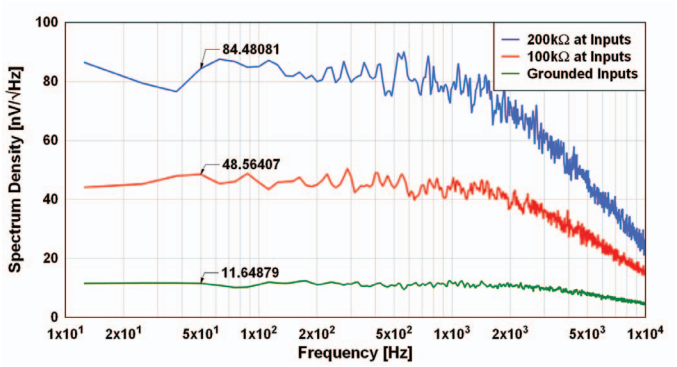

Fig. 14. Input noise spectral density (channel # 0): shorted input, $100k\Omega$ and $200k\Omega$ connected to the inputs

It is worth to mention that designed IC is a part of the project demonstrator targeted for substances identification using THz spectroscopy. This device is being developed and supposed to contain - apart from electrical parts - also several mechanical components, like sample feeder.

Acknowledgment

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