The Integrated Selective Readout Amplifier for NMOS THz Detectors

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***Abstract*—This paper presents design and measurement of the integrated readout circuit for NMOS THz detectors. This work is a direct continuation of the previous design, described in [1]. The main improvement - with respect to the former IC - is a modification in the AC amplifier structure. The new circuit still bases on a chopper amplifier architecture, but the selective AC amplifier is used to gain the modulated signal. This results in significant improvement of noise parameters. Designed structure was fabricated in AMS C35 process and measured in the dedicated testing environment.**

***Index Terms*—Teraherz Detector, Selective Amplifier, Chopper Amplifier, Transconductor, Gm-C Filter, AMS C35.**

I. Introduction

In recent years silicon metal-oxide-semiconductor field-effect transistors (MOSFETs) have gained much attention for THz detection [2], [3], [4]. Also presented readout circuit is dedicated for NMOS-based THz detectors, described in [5] and [6]. According to information mentioned previously in [1], such a readout circuit is mainly low-noise, small DC signal amplifier with wide-range gain control. The measurements of prototypes of the first readout circuit proved that the chopper amplifier architecture was the right choice, but the entire circuit suffered from the relatively high noise level at the output. Hence, the improvement of noise properties was the main aim of the second version design.

In previously designed chopper amplifier the AC gain stages placed in between the modulator and demodulator block have a flat transfer characteristic in a frequency range from DC to approx. 2 MHz. But it is important to notice that the useful information is carried only by signal components of the switching (modulation) frequency (1 kHz) and a few of its harmonics. Because of that, the low-side and high-side bandwidth limitation, applied to the AC amplifier, should result in elimination of a significant portion of unwanted signals (i.e. amplified interferences from the input, noise signal of the amplifiers) and thus, improvement of the noise parameters of the entire readout amplifier.

As a proof of concept, dedicated test board was designed. It was decided to use some internal blocks of the first version of the readout IC and extend it with some external components connected at the PCB level rather than build the entire circuit starting from scratch. After the modulator and the first gain stage signals from the IC were connected (by built-in buffer and diagnostic outputs) to the external AC amplifier. This amplifier was built of two sections of LP and HP active filters and it passed the fundamental frequency of the modulator and up to its third harmonics. Demodulation process was performed also at the PCB level, in similar way as the modulation is done inside the IC - using the CMOS switches. The complementary outputs of the demodulator were subtracted, the remaining components of the switching frequency were eliminated by a LP filter, and resulting DC signal was buffered and sent to the output. The circuit concept described above is presented schematically in Figure 1.

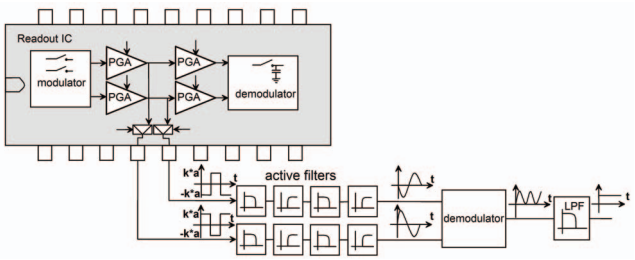

Fig. 1. The schematic view of the integrated chopper circuit with external, selective AC amplifier

The switching (modulation) frequency was increased to 200 kHz, what makes the values of all passive components (especially capacitors) easily implementable inside the second version of integrated readout circuit. The tests performed in target application (i.e. with NMOS-based detector illuminated with THz radiation) proved the concept of selective AC amplifier - the output noise level was significantly reduced with respect to the first version of the readout circuit.

Due to promising results of described experiment, it was decided to commence the design of the readout circuit improved version.

II. Improved Readout Architecture

This section includes detailed readout circuit description with particular emphasis placed on improvements introduced in respect to the previous version. As it was mentioned in abstract, main changes have been made in AC amplifier architecture, but the structure of demodulator has also been

modified. Figure 2 shows the schematic view of improved chopper amplifier.

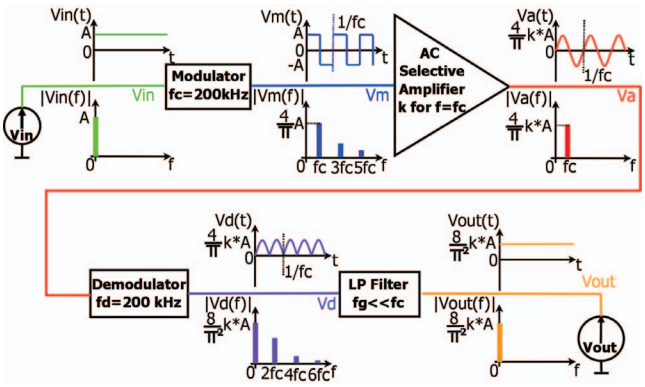

Fig. 2. Improved architecture of designed chopper amplifier with signals in time and frequency domains

The idea of modified readout architecture bases on concept described in [7]. At the circuit input, DC signal with the magnitude A and single frequency component in $f = 0$ is applied to the modulator block. As a result of modulation, its spectrum is convoluted with a square wave spectrum and produced signal, with trigonometric Fourier series expansion given by equation (1).

$$U_m(t) = \sum_{l=1}^{\infty} \frac{2A(1-(-1)^l)}{l\pi} \sin(l\pi t) \tag{1}$$

Modulated signal is then applied to the AC selective amplifier. In perfect, theoretical situation, only the frequency component $f = f_c$ is amplified (with k gain), the other ones are entirely suppressed.

Demodulation process is made by a circuit similar to the modulator (built of CMOS switches), but this time the square wave is convoluted with a sine signal (not a DC one). As a result of this operation, a rectified sine wave is produced, with trigonometric Fourier series expansion given by (2).

$$U_d(t) = \frac{8kA}{\pi^2} - \sum_{l=2,4,6\ldots}^{\infty} \frac{16kA}{\pi^2(l^2-1)} \cos(l\pi t) \tag{2}$$

Then, the LP filter with cut-off frequency $f_o << f_c$ passes only the DC component of this rectified signal.

At the end, output wave is a DC signal with $\frac{8A}{\pi^2}k \simeq 0,81Ak$ magnitude, where A is an input magnitude and k is the gain of the AC amplifier for f_c frequency. Due to this bandwidth limitation the noise level at the output should be considerably reduced.

A. Modulator/Demodulator

Schematics of modulator and demodulator circuits are similar, based on switching architecture shown in Figure 3.

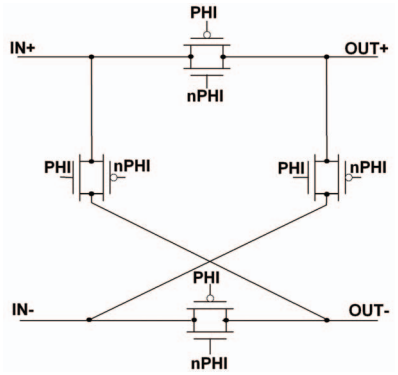

Fig. 3. Modulator and demodulator architecture

The only difference between them consists in transistors dimensions. In modulator, devices with minimal length and width have been used to minimize the *charge injection* effect. This phenomenon, shown in the Figure 4, is related to channel charge of the FET exiting through its source and drain terminals during the switching-off process.

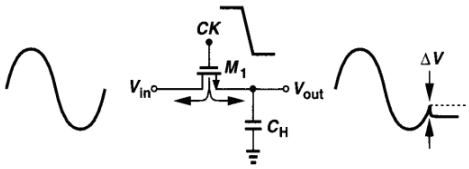

Fig. 4. Charge injection phenomenon [8]

If in the circuit presented in Figure 4 the entire channel charge is injected in equal ratio to the S and D terminals of the switching FET, the amplitude of output signal distortion (spike) is given by equation (3) [8].

$$\Delta V = \frac{WLC_{ox}(V_{DD} - V_{in} - V_{th})}{2C_H} \tag{3}$$

In the chopper amplifier architecture used in designed circuit these peaks deform the input signal for the AC amplifier and cause additional, unwanted frequency components. Due to working with very small signals, minimization of this effect is extremely important. Taking into account these requirements, given in equation (3), transistors with minimum dimensions have been used in modulator.

B. Selective AC Amplifier

The main goal of the AC amplifier is to provide high, variable gain for frequency $f = 200\ kHz$ and strong suppression outside this band. Due to this fact, AC amplifier circuit has to be based on band-pass filter architecture. There are three main types of this kind of device: Continuous-Time Filters, Switched-Capacitor Filters and Digital Filters. The last two solutions produce interferences specific for digital circuits (e.g.

propagating by substrate coupling), so it has been decided to base on C-T filter architecture - or rather to be precise - on $G_m - C$ filter.

$G_m - C$ biquad section built of four transconductors and two capacitors is shown in Figure 5.

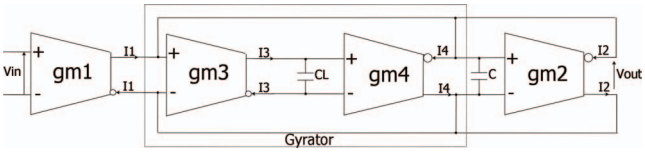

Fig. 5. Pass band biquad section

Trancondutors gm3 and gm4 form the gyrator circuit loaded by the C_L capacitor. Under these conditions gyrator transforms capacitance C_L into some L_z inductance, according to the equation (4):

$$L_Z = \frac{C_L}{g_{m3} \cdot g_{m4}} \tag{4}$$

This simulated inductance forms together with capacitance C a LC circuit with the f_0 resonant frequency. Transconductors gm1 and gm2 are used as input/output buffers, their transconductances ratio determines the gain for f_0. Main parameters of presented biquad section are described by equations (5-7).

$$\omega_0 = \frac{1}{\sqrt{L_Z C}} = \sqrt{\frac{g_{m3} \cdot g_{m4}}{C_L \cdot C}} \tag{5}$$

$$Q = \frac{\sqrt{C}}{\sqrt{L_Z} \cdot g_{m2}} = \frac{\sqrt{g_{m3} \cdot g_{m4}}}{g_{m2}} \cdot \sqrt{\frac{C}{C_L}} \tag{6}$$

$$k(\omega = \omega_0) = \frac{g_{m1}}{g_{m2}} \tag{7}$$

Schematic of single transconductor is shown in Figure 6.

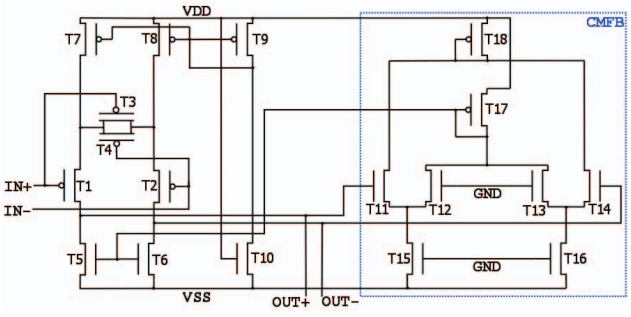

Fig. 6. Schematic of the transconductor cell

T1 and T2 are just a differential pair with T5, T6 operating as active load and T7, T8, T9 as current source. T10 is used to set the current for those transistors, T11-T18 are a Common Mode Feedback (CMFB) block, controlling the common mode voltage at circuit outputs. T3 and T4 form a specific resistor controlled by input voltage. Both transistors operate in triode region, and implement dynamic linearization of circuit I-V characteristic: when differential input voltage increases, transconductances of T1 and T2 decrease, but it is compensated by drop in r_{ds} value of T3 and T4. Linear I-V characteristic for wide input range means constant transconductance value. This is an extremely important issue for g_m-cells used in biquad section, because values of their transconductances define circuit parameters (equations (5-7)).

Assuming ideality of CMFB, current mirror and active load, transconductance of circuit presented in Figure 6 is described by equation (8) [9].

$$G_m = \frac{2K_{1,2}}{\alpha\sqrt{\frac{2I_{DS}}{K_{1,2}} - \frac{8U_i^2}{\alpha^2}}}\left(\frac{I_{DS}}{K_{1,2}} - \frac{8U_i^2}{\alpha^2}\right) \tag{8}$$

where $\alpha = 1 + \frac{K_{1,2}}{4K_{3,4}}$,
$K_i = \frac{1}{2}\mu C_{ox}\frac{W_i}{L_i}$,
U_i is differential input voltage,
I_{DS} is DC current of T1/T2.

The wide-range gain control is achieved by four identical biquad sections connected in series using multiplexers. This configuration is presented in Figure 7.

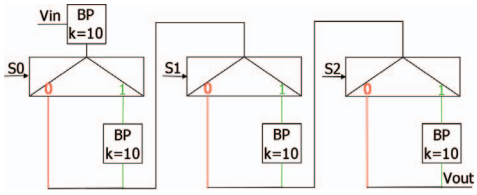

Fig. 7. AC amplifier structure

There are three control signals: S0, S1 and S2. If any of them is set to 1, the corresponding biquad section is connected to the signal path. Otherwise this section is shorted to ground and signal path is just wired to the next multiplexer. Since the gain of all band pass filters is set to 10 (for $f_0 = 200\ kHz$), it is possible to achieve the 10/100/1000 or 10 000 gain for the entire AC amplifier.

C. Low Pass Filter

As it was mentioned before, LP filter has cut-off frequency significantly lower than chopping frequency $f_c = 200\ kHz$, so it converts rectified sine wave into a DC signal. Designed filter is based on unity-gain Sallen-Key low-pass architecture, which is presented in Figure 8.

This architecture has been described in detail in [10]. If $R_1 = R_1' = R_2 = R_2' = R$ and $C_1 = C_1' = C_2 = C_2' = C$, then cut-off frequency is given by the well-known relation $f_0 = \frac{1}{2\pi RC}$. In designed filter $R = 2\ M\Omega$ (used high-resistive polysilicon) and $C = 16.6\ pF$, what results in $f_0 \simeq 4.783\ kHz$.

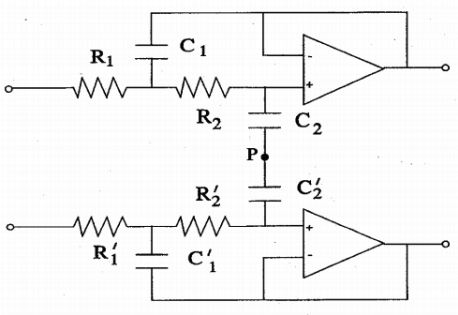

Fig. 8. Differential low pass filter [10]

D. Chip Layout

Designed structure was fabricated in AMS C35 process, layout is presented in Figure 9 (2.44 X 2.44 [mm]).

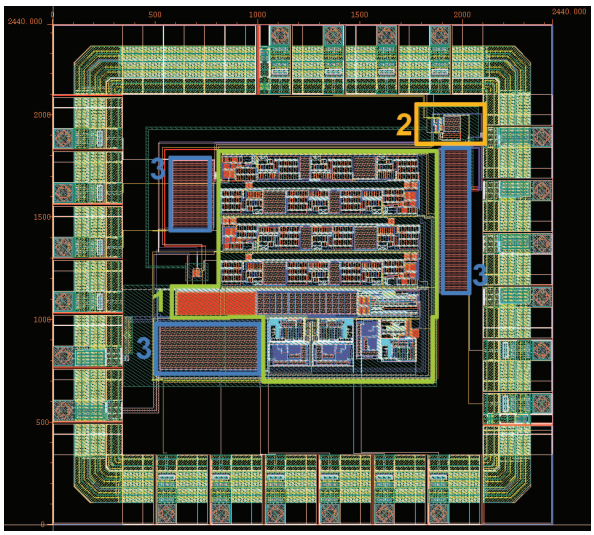

Fig. 9. Designed structure

The main part of the chip contains designed chopper amplifier circuit and is marked as 1. Number 3 denotes the internal supply decoupling capacitors. Number 2 in Figure 9 is a square wave generator (built of three inverters, two resistors and capacitor) producing control signals for modulator and demodulator. These two circuits can be also controlled by external signals, by means of dedicated inputs, at that time power supply for internal generator is turned off. Because of interferences generated by this circuit, its layout has been isolated from other structures and surrounded by guard rings. For the same reason all switching devices have separate power supply and ground ports.

III. Simulation Results

In this section several simulation results are presented. Figure 10 shows transfer characteristic for designed AC amplifier.

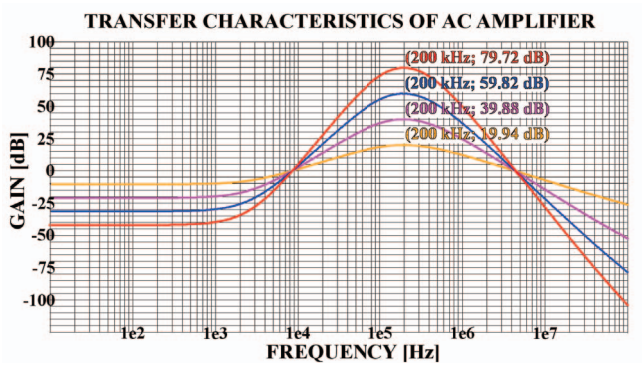

Fig. 10. Characteristic of AC amplifier for different numbers of biquad sections filters turned on

Figure 11 presents transfer characteristic for whole chopper amplifier, 12 shows results of noise analysis.

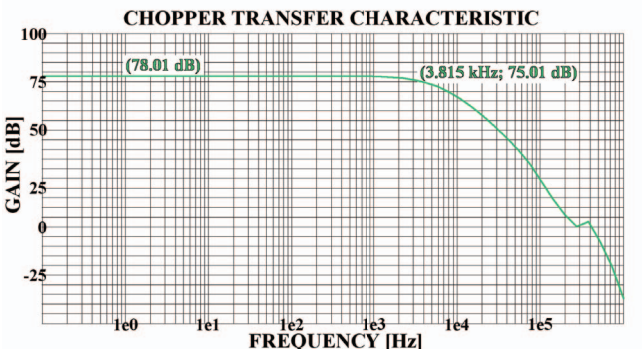

Fig. 11. Transfer characteristic of designed chopper amplifier for maximum gain

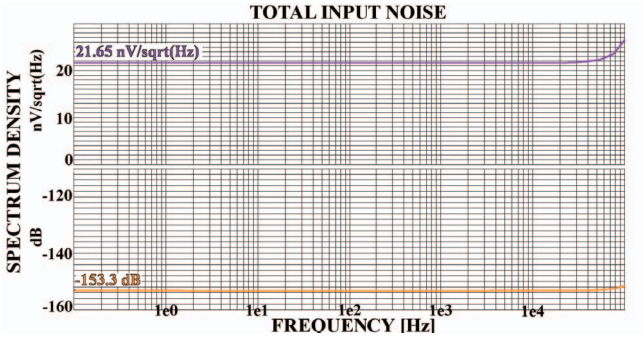

Fig. 12. Input noise characteristic of designed chopper amplifier

It is important to notice, that there is no 1/f noise influence in characteristic in Figure 12. That fact confirms one of the main advantages of chopper amplifier architecture - 1/f noise cancellation (because only AC component is amplified).

IV. Measurements

Two different test setups were designed to enable two different kinds of measurements to be performed on manufactured ICs - characterization and tests in target application.

A. Prototypes Characterization

The first test setup was intended to be used for full characterization of prototypes - precise determination of their parameters for all modes of operations (i.e. with internal and external clocking signals for modulators, for different gains), noise measurements and other specific tests. Taking into account the need of studies to be performed with very small signals, the special attention was paid for proper shielding, elimination of interferences coming from outside of the test environment and also ones generated inside e.g. by switching circuits. For that purpose the test setup is constructed in a form of a complete device with shielding enclosure, containing all the circuit elements located at dedicated PCB. To avoid the interferences conducted from power line it was decided to use the battery supply - to place two Li-Ion cells inside the enclosure too. The positive and negative supply of the IC under test and cooperating elements is obtained using two linear LDO regulators, located at the PCB together with battery loader circuit. The PCB is designed in a way to separate the elements of the sensitive input signal path from the output signal buffers and components of external clocking generator. Besides, the supply tracks are routed and decoupled separately for two mentioned sets of supply pins of the IC - signal part and the switching part, the output buffers and external generators have also the separate power paths. The last mentioned block, as the suspected source of interferences is placed at the opposite side of the PCB in respect to signal path elements and shielded with the metal fill layer located above and cut with a slot to direct the current flow. For the same reason the connection to the external potentiometer of the on-chip oscillator is made with shielded twisted-pair cable. The potentiometer together with switches selecting the clocking signals for modulator and demodulator are soldered within additional shielding enclosure inside the main one (shield inside a shield). Besides, the external clocking signal generators are turned off whenever the internal source of control signals is selected. The internal harness of the test setup is connected to the PCB by means of multipin connectors to allow the easy removal of the board for changing the circuit components (e.g. the input divider). The four BNC sockets allow to monitor the internal signals of the IC (before the demodulator, after the demodulator, after the LP filter), the final output (DC) and internal control signal for modulator / demodulator. The four mentioned signals paths from the inside of the test IC are not routed directly to the sockets, but are buffered by low-noise operational amplifier. There are some optional passive elements footprints placed on a PCB in a signal path of the buffering amplifier. In this way the additional LP or HP filtering and / or signal amplification can be easily introduced in case of any need caused by measurement environment. The test setup used for prototypes characterization is presented in Figure 13.

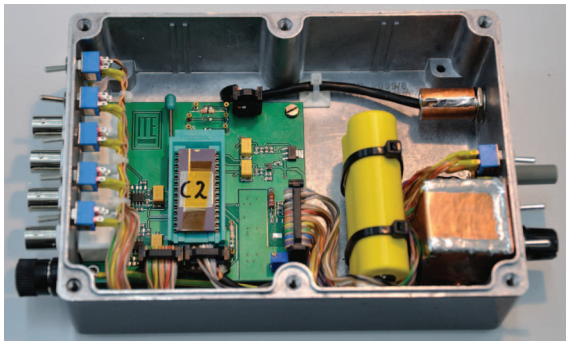

Fig. 13. The test setup for prototypes characterization

The measurements started with testing the demodulator and LP filter blocks. The first of them rectifies sine wave, second one transmits only DC component of the signal. These operations are presented in Figure 14.

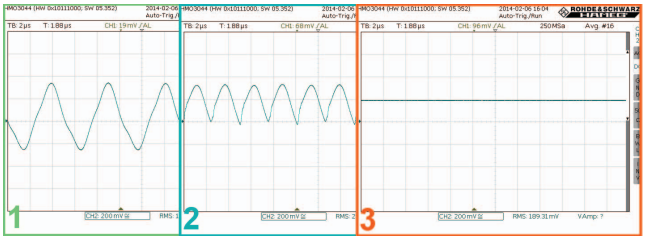

Fig. 14. Signal before demodulator (1), between demodulator and LP filter (2) and after LP filter (3)

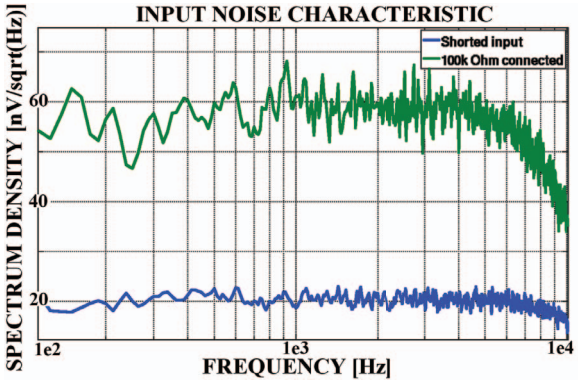

Fig. 15. Input noise spectral density for shorted input (blue) and connected 100 $k\Omega$ resistor (green)

Figure 15 shows results of input noise measurement performed twice: with input shorted to ground and with resistor 100 $k\Omega$ connected to it.

It should be noted that spectral density for shorted input matches simulation results showed in Figure 12. Also noise level equivalent to the thermal noise of used resistor is consistent with theoretical equation $\bar{u}^2 = 4k_BTR\Delta f$.

B. Measurements with THz source

At the laboratory of the Institute of Optoelectronics, Warsaw Military University of Technology series of other kind experiment was performed - measurement of the readout IC in target application, i.e. with NMOS-based detector at the input. Deployed detectors were manufactured in ITE proprietary CMOS process within the frame of former research project. This kind of investigations required another test setup to be constructed in a form of complete, compact device fitting into the optical lane. The small-form shielding enclosure was utilized as mechanical basis for circuits elements. At the bottom of the box the Li-Ion rechargeable battery set is placed, used as power source for device. Above bateries two PCBs are located one above the other, contacted together with multipin connector. The lower PCB contains the voltage regulators and generators of the clocking signals for modulator and demodulator blocks, while the upper PCB groups the THz detector chip, the IC under test, the output buffers and other elements needed to build the application circuit. The whole wiring inside the enclosure is routed to the lower PCB to allow easy dismounting of the upper PCB. Thanks to this modular design the upper PCB, containing detector and IC under test can be replaced in convenient way to explore different concepts of application circuits. To allow the THz beam to illuminate the detector, the hole is drilled in the top cover of the enclosure.The surface of this cover is coated with ani-ESD conductive foam to suppress any interferences of THz wave possible in the lane.

Figure 16 presents used testing environment, Figure 17 shows some measurement results. The THz source used in experiments produced 340 GHz radiation, chopped (modulated) with 45.83 Hz. The gate-source voltage of detecting NMOS FET was set to 1.32 V, close to its threshold voltage.

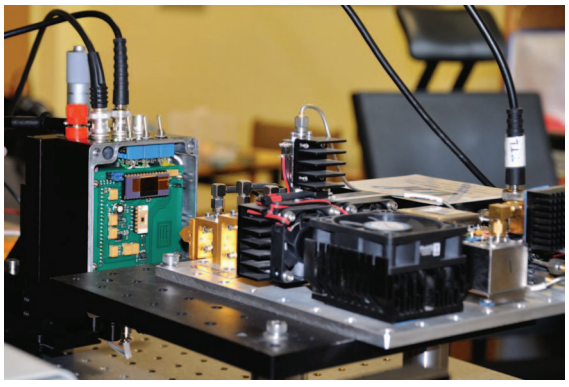

Fig. 16. Testing environment

Waveform after AC amplifier is a carrier signal ($f = 200\ kHz$) modulated with amplitude of the input signal ($f = 45.83\ Hz$). Amplitude of this carrier is related to the input voltage offset of the chopper amplifier, which should not exceed 100 μV.

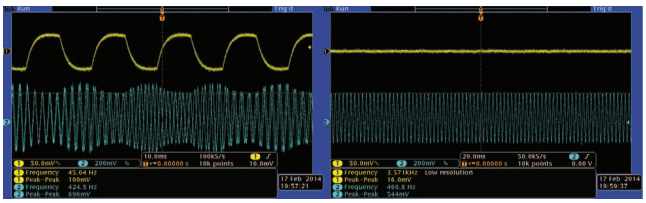

Fig. 17. Measurement using THz source: output signal (yellow) and after AC amplifier (blue) for irradiated (left) and covered (right) detector

V. Conclusions

The performed measurements match the simulation results and confirm proper operation of designed chopper amplifier in a test setup used for characterization as well as in target application. The main goal: minimization of noise level has also been reached - input noise density is about 20 $\frac{nV}{\sqrt{Hz}}$ and 1/f noise has been significantly reduced.

The next works assume developing of spectrum analyzer prototype: several detectors - each one designed for different frequency - will be placed in line and connect to the individual readout circuits.

Acknowledgment

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